REMARKS

In response to the Office Action mailed February 7, 2006, The Applicants respectfully request reconsideration. To further the prosecution of this Application, the Applicants submit the following remarks, have amended claims, and have added claims. The claims as now presented are believed to be in allowable condition.

Claims 1-10 and 39-41 were pending in this Application. By this Amendment, claims 42-50 have been added. Accordingly, claims 1-10, and 39-49 are now pending in this Application. Claims 1 and 41 are independent claims.

Claim Amendments

Independent claims 1 and 41 have been amended to clarify the nature of the invention. By this amendment, claims 1 and 41 recite the solder fusing stage as comprising "a metallic stencil, an applicator operable to apply a paste containing the flux and the solder onto the set of circuit board pads through the metallic stencil, and a squeegee operable to remove paste from the metallic stencil." Support for the recitation of the metallic stencil can be found in the Specification, for example, on page 12, lines 19 through 28. Support for the recitation of the applicator can be found in the Specification, for example, on page 13, lines 14 through 21. Support for the recitation of the squeegee can be found in the Specification, for example, on page 13, lines 16 through 18. The amendments to the claims do not add new matter to the application.

Also, claims 3-5 were amended to address antecedent basis issues raised by the amendment to claim 1. No new matter has been added to the application by theses amendments.

Initial Matters

On June 26, 2003, the Applicants submitted formal drawings for the present application. The Office Action mailed February 7, 2006 does not indicate whether or not the drawings were accepted or objected to. The Applicant respectfully request clarification regarding this issue.

Rejections under §102 and §103

Claims 1-9 and 39-41 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,866,475 (Yanagida). Claim 10 was rejected under 35 U.S.C. §103(a) as being unpatentable over Yanagida in view of U.S. Patent No. 2,933,412 (Thayer). Claims 6-8 were further rejected under 35 U.S.C. §103(a) as being unpatentable over Yanagida in view of U.S. Patent No. 5,866,475 (Lawler).

The Applicants respectfully traverse each of these rejections and request reconsideration. The claims are in allowable condition.

The Office Action has rejected independent claims 1 and 41. Taking amended claim 1 as an example, the claim relates to a circuit board processing system that comprises a circuit board fabrication stage, a solder fusing stage, and a washing stage. As recited, the circuit board fabrication stage is configured to fabricate a circuit board having a set of circuit board pads. The solder fusing stage is coupled to the circuit board fabrication stage and is configured to (i) apply flux and solder concurrently to the set of circuit board pads, and (ii) activate the flux and melt the solder to form a set of substantially flat solder coatings which is fused to the set of circuit board pad. The solder fusing stage also comprises a metallic stencil, an applicator operable to apply a paste containing the flux and the solder onto the set of circuit board pads through the metallic

stencil, and a squeegee operable to remove paste from the metallic stencil. The washing stage is coupled to the solder fusing stage and is configured to remove contamination from a surface of the circuit board having the circuit board pads and from the set of substantially flat solder coatings which is fused to the set of circuit board pads.

Yanagida discloses a method for forming solder bumps (Title). In Yanagida's description of the related art, Yanagida explains that, in order to form a solder bump, an electrode pad 12 composed of an Al alloy or the like is formed on a silicon substrate 10 by a sputtering method, and then a surface protective layer 11 composed of an insulating film such as polymide film and silicon nitride film is coated on the substrate 10 (column 1, lines 41-46 and Fig. 7A). Then, an opening is formed in the surface protective layer 11, thereby to form a connecting hole for exposing the electrode pad 12, and a Ball Limiting Metal (BLM) film 14 composed of a barrier metal layer is formed with patterning on the electrode pad 12 thereafter (column 1, lines 46-50). Next, a resist film 18 is formed on the substrate, and is applied with patterning further so as to form an opening portion 16 where the BLM film 14 is exposed (column 1, lines 51-54 and Fig. 7B). Next, a solder film 20 is formed on the substrate by vapor deposition or the like (column 1, lines 55-56 and Fig. 7C). In succession, the resist film 18 is removed by resist peeling and cleaning, and the solder film 20 on the resist film 18 is lifted off at the same time (column 1, lines 56-59). As a result, the solder film 20 remains behind only in the opening portion 16 (column 1, lines 59-61 and Figs. 7B and 7D). Next, the solder film 20 is dissolved by heat treatment, and the solder film 20 located on the BLM film 14 is transformed into ball-shaped solder, thus forming a solder ball bump 22 (column 1, lines 62-65 and Fig. 7E).

Independent claims 1 and 41 were rejected under 35 U.S.C. §102(b) as being anticipated by Yanagida. However, Yanagida does not teach or disclose

all of the elements of the Applicants' amended claims 1 and 41 and as such, claims 1 and 41 patentably distinguish over Yanagida. Specifically, Yanagida does not teach or suggest a solder fusing stage that comprises a metallic stencil, an applicator operable to apply a paste containing the flux and the solder onto the set of circuit board pads through the metallic stencil, and a squeegee operable to remove paste from the metallic stencil, as claimed by the Applicants.

As indicated above, Yanagida discloses the use of a resist film 18, applied with a patterning on a substrate, to form an opening 16 where a BLM film 14 is exposed. Then in Yanagida, a solder film 20 is formed on the substrate by vapor deposition, the resist film 18 is removed, and the solder film 20 remains behind in the opening 16. There is no teaching or suggestion in Yanagida of a metallic stencil or an applicator operable to apply a paste containing the flux and the solder onto the set of circuit board pads through the metallic stencil. Yanagida merely teaches of the use of a solder film. Furthermore, it is unclear how one could modify Yanagida to print paste onto the set of circuit board pads through a metallic stencil. In particular, Yanagida deals with packaging a semiconductor device on mounting substrate (e.g., see column 1, lines 5-10 of Yanagida), not mounting a circuit board package on a circuit board.

Additionally, Yanagida does not teach or suggest a squeegee operable to remove the paste from the metallic stencil, as claimed by the Applicants. Yanagida merely discloses removal of the resist film by resist peeling and cleaning. There is no teaching or suggestion in Yanagida of the removal of paste from the solder film using a squeegee.

For the reasons stated above, claims 1 and 41 patentably distinguish over the cited prior art, and the rejection of claims 1 and 41 under 35 U.S.C. §102(b) should be withdrawn. Accordingly, claims 1 and 41 are in allowable condition.

Because claims 2-10, 39-40, and 42-44 depend from and further limit claim 1 and claims 45-49 depend from and further limit claim 41, claims 2-10, 39-40, and 42-49 are in allowable condition for at least the same reasons.

Dependent claim 10 was rejected under 35 U.S.C. §103(a) as being unpatentable over Yanagida in view of Thayer. Claims 6-8 were further rejected under 35 U.S.C. §103(a) as being unpatentable over Yanagida in view of Lawler. However, because these claims depend from allowable independent claim, the rejection is moot.

New claims

Claims 42-50 have been added to the application by this amendment. Claims 42-44 depend from claim 1 and claims 45-49 depend from claim 41. Support for claims 42 and 47 can be found in the Specification, for example, on page 14, lines 7-9 and in Fig. 3. Support for claims 43 and 48 can be found in the Specification, for example, on page 20, lines 16-27 and in Figs. 8 and 9. Support for claims 44 and 49 can be found in the Specification, for example, on page 16, lines 23-28. Support for claims 44 and 45 can be found in the Specification, for example, on page 19, lines 20-22. Support for claim 50 can be found in the Specification, for example, on page 13, lines 13-16. The new claims do not add new matter to the Application.

Conclusion

In view of the foregoing remarks, this Application should be in condition for allowance. A Notice to this affect is respectfully requested. If the Examiner believes, after this Response, that the Application is not in condition for allowance, the Examiner is respectfully requested to call the Applicants' Representative at the number below.

The Applicants hereby petitions for any extension of time which is required to maintain the pendency of this case. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 50-3661.

If the enclosed papers or fees are considered incomplete, the Patent Office is respectfully requested to contact the undersigned collect at (508) 616-2900, in Westborough, Massachusetts.

Respectfully submitted,

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